JSS Mahavidyapeetha

JSS Academy of Technical Education, Noida

Department of Electronics & Communication Engineering.

FACULTY PROFILE

1. Personal Details

NAME	**Mr. SAMPATH KUMAR V**
DEPARTMENT	ELECTRONICS & COMMUNICATION ENGINEERING
DESIGNATION	ASSISTANT PROFESSOR
PHONE	-
EMAIL ID	Sampath.kumarjss@jssaten.ac.in
Date of Joining (JSSATEN)	30.09.2002

2. Experience

Total Experience in Years: 23.6	Teaching: 20	Industry: 3.6	Research: -

3. Qualifications

COURSES	SPECIALIZATION	Year of Award	INSTITUTION	UNIVERSITY
B.E.	Electronics & Communication Engineering	1998	SJMIT – Chitradurga, Karnataka	Kuvempu University - Karnataka
M.Tech.	VLSI Design	2007	UPTU – Lucknow	UPTU - Lucknow
Ph.D.	Memory Design		CDAC, Noida	AKTU - Lucknow
Post Doc.	-	-	-	-

4. Research & Publications

Papers Published in Web of Science indexed Journals	03	
Papers Published in SCOPUS indexed Journals	09	
Papers Published in other Journals	10	

Papers Presented in Conferences / Symposium	15	
Books / Book chapters Published	03	
	Name of the book: 8051 Microcontroller, Microcontroller and Embedded System Publisher: KATSON Year of Publication: 2016, 2012. 2011	

5. Research Guidance

PhD Guide? Give field & University	NO	NA
Ph.D.s / Projects Guided	Ph.D. Awarded: Guiding:	Projects at Master's Level: Projects at Bachelor's Level:

6. Grants

i. Funds Received (Projects)

Project Name	Grant Amount	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
AICTE IDEA Lab 2021	Rs. 110 Lakhs	14.06.2021	5 Years	IDC Cell, AICTE, New Delhi
Design and development of PCB prototype machine with eCAD interfacing and 3D Printer	Rs. 3.25 Lakhs	2017	3 Years	VRPS Scheme, AKTU, Lucknow

ii. Patents

Sl. No.	Title Details	Details of award of patent / Filed
1	Optimal Intelligent Controlling and Management of Electrical Vehicle	Application No. 202211007129 A dt. 25/02/2022
2	Printed Circuit Board (PCB) Prototyping using Layout Aware Probing	Application No. 202011033134, TEMP/E-1/36841/2020-DEL, on 02/08/2020.
3	Method for Welding Polypropylene Polymer using Nitrogen Gas	Application No. 202011033133, TEMP/E-1/36840/2020-DEL on 02/08/2020.

4	The Novel Low Power SRAM Core Cell	No: C-DAC/IPR/IDF/28-11-2011) – Application No - 3062/DEL/2013 – Date: 15/10/2013.

iii. Consultancy

Title of the work	Amount in Rs.	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
-	-	-	-	-

7. Awards Received

Awards	1. Received a best paper award in ICTIEE2022 9th International conference on Transformations in Engineering Education in the track Student Centered Learning Environment organized by IUCEE on January 7th - 9th 2022. 2. Received an Innovation Ambassador (Advanced Level) certificate from MoE's Innovation Cell (MIC), Govt. of India for the Academic Year 2021. 3. Received an Innovation Ambassador certificate from MoE's Innovation Cell (MIC), Govt. of India for the Academic Year 2020. 4. Institute Innovation Cell, Convener under Ministry of Education, GoI received a 4.5 Golden Star rating for the Academic Year 2020. 5. Institute Innovation Cell, Convener under Ministry of Education, GoI received a 4.0 Golden Star rating for the Academic Year 2019. 6. Received an appreciation letter for the contribution of Innovation Cell activities for the Academic Year 2018, 2019 & 2020. 7. Received a Certificate of Membership from MHRD's Innovation Cell for the contribution of Institution Innovation Council at JSSATE, Noida as a Convener for the academic year 2018-19. 8. Received certificate of appreciation for invited talk on "Attainment of CO's, PO's & PSO's using direct and indirect tools" in the National Workshop on Importance of Accreditation for Technical Education and Development of SAR on July 31 – August 01 2019, Assam Science and Technological university, Guwahati, Assam under TEQIP III project of MHRD, New Delhi. 9. Received an "BEST PAPER AWARD "at BBDIT - NATIONAL CONFERENCE – 2007 10. Received an Appreciation letter from JSSATE – Director for best Teaching - 2008. 11. Received an Appreciation letter from JSSATE – HOD (Mechanical Department) for successful completion of UP Technical University end semester examination – 2004/05.

8. Publications

i. Monogram:

1. "Design of Reconfigurable Decoder for SRAM – Schematic and Layout Design of 5:32 bit reconfigurable decoder" – LAP LAMBERT Academic Publishing.

ii. Journals

1. An Invasive Weed Optimization for Sensor Less Control of Grid Integrated Wind Driven Doubly Fed Induction Generator, Journal: IEEE Access, Volume:10, pp 109082-109096, doi:0.1109/ACCESS.2022.3213982, 2022.

2. Multilevel Cascaded Inverters having Improved Output Level with Reduced Power Switches - A Novel, GRENZE International Journal of Engineering and Technology, Volume-8, Issue-1, Pages 542-551,2022.

3. Competency Based Education and Continuous Assessment in Laboratory to acquire higher order learning levels: Challenges, Process and Outcomes, Journal of Engineering Education Transformations, Volume No 35, January 2022, Special issue 1, pp: 187-193

4. "VLSI systems energy management from a software perspective – A literature survey", Journal of perspectives in Science (2016), Elsevier, Vol -8, pp 611-613.

5. "Energy efficient and high-speed domino logic circuits ", Int. Journal of Engineering Research and Applications, ISSN: 2248-9622, Vol. 5, Issue 4, (Part - 1) April 2015, pp.36-39.

6. "Automated Multimode Smart Charger with Power supply control to ensure uninterrupted power backup" , ISSN :2321-5984, Vol-3, Issue 7, IIJEC, July 2015.

7. "Voltage Mode Third Order Quadrature Oscillator", ISRN Electronics Volume 2014 Article ID 126471 (Hindawi Publishing Corporation)

8. "Reduction of Sub-threshold Leakage Current in MOS Transistors" – World Applied Sciences Journal 25 (3): 446-450, 2013.

9. "Explicit timing analysis of discontinuous RC global VLSI interconnect lines under ramp input" – Journal of Electron Devices, Vol.15, 2012, pp. 1249 – 1253. (TAYLOR & FRANCIS LTD)

10. "Performance analysis of narrowband and wideband LNA's for Bluetooth and IR-UWB" – IJSRD, Vol2, Issue3, Nov 2014.

11. "Design of a current mode sample and hold circuit at sampling rate of 150 MS/s" – IJERA, Vol4, Issue 10, Nov 2014.

12. "Delay Minimization of 3 Cascaded Inverters with the Help of Logical Effort and Transistor Sizing" Journal of VLSI Design Tools & Technology, Vol 2, No 1 2012.

13. “Characterization and Comparison of Low Power SRAM Cells” – Journal of Electron Devices, Vol.11, 2011, pp.560-566. (TAYLOR & FRANCIS LTD)

14. “Comparative study of Different sense amplifiers in submicron CMOS Technology” – IJAET, Vol.1, Issue 5, Nov 2011, pp.342-35.

15. “Deep sub-micron SRAM design for DRV analysis and low leakage” - IJAET, Vol.1, Issue 5, Nov 2011, pp.429-436.

16. “Design of 1-bit full adder for low power applications” – IJAEST, Vol No.10, Issue No.1, Sept 2011 pp.019-025.

17. “An adiabatic approach for low power full adder design” – IJCSE, Vol.3, No.9, Sept 2011, pp.3207-3221.

18. “Reducing power in different technologies using FSM architecture” - IJ of VLSI Design & Communication Systems (VLSICS), Vol.2, No.3, Sept -2011, pp.243-251.

19. “Design and Implementation of ATD for 100MHz SRAM in 130nm” – Journal of AIP, Vol – 1324, P-No- 369 – 372. May 2010.

iii. Conferences

International:

1. The novel evaluation scheme for competency-based learning, authentic assessment and its implementation strategies for universities of higher education, 10th International Conference on Transformations in Engineering Education, ICTIEE 2023, held at Vidyavardhaka College of Engineering, Mysuru in association with IUCEE from January 5- 8, 2023.

2. Competency based education and continuous assessment in laboratory to acquire higher order learning levels: Challenges, Process and Outcomes, 9th International Conference on Transformations in Engineering Education, ICTIEE 2022, 7^{th} – 9^{th} Jan 2022.

3. Multilevel Cascaded Inverters Having Improved Output Level with Reduced Power Switches- A Novel Approach, ETCAN’21,

4. Estimation of power and delay parameters for reconfigurable decoders in SRAM by selective pre-charge schemes" in the 2020 IEEE 5th International Conference on Computing, Communication and Automation (ICCCA), Jointly Organized by Aurel Vlaicu University of Arad, Romania & Galgotia University, India.

5. "Control techniques analysis to find effectiveness of suppressing output voltage total harmonic distortion for fuzzy based single-phase voltage source inverter",

International Conference" on “Intelligent Control and Computation for Smart Energy and Mechatronic System (ICCSEMS-2020) at JSS Academy of Technical Education, Noida.

6. “Estimation of power and delay dependent parameters in reconfigurable decoders for selection of SRAM by means of configurable selective pre-charge schemes”, International Conference on Contemporary Computing and Applications on 05 - 07 February 2020, Dr. A.P.J. Abdul Kalam Technical University, Lucknow.

7. “Low power technique in domino logic circuit”, ICRITO 2015, AMITY – Noida, Sept 2-4, 2015.

8. "Analysis of Energy Efficient PTL based Full Adders using different Nanometer Technologies” - IEEE -2nd International Conference on Electronics and Communication Systems (ICECS) – Coimbatore, India. 26 Feb – 27 Feb 2015.

9. “Analysis of Low Power 1-bit Adder Cells using different XOR- XNOR gates” - IEEE International Conference on Computational Intelligence and Communication Technology (CICT-2015) – ABES – Ghaziabad, India. 13 Feb – 14 Feb 2015.

10. “Elmore’s approximations based explicit delay and rise time model for distributed RLC on-chip VLSI global interconnect” – IEEE Symposium on Humanities, Science and Engineering Research, 2012. Kuala Lumpur, Malaysia

11. “Closed form expressions for extending step delay and slew metrics to ramp inputs for on-chip VLSI RC interconnect” – Springer & ACEEE, Control, Communication and Power Engineering CCPE -2012, April 27-28, 2012, Bangalore.

12. “Design of Ternary Content Addressable Memory (TCAM) With 180 NM “International Conference on Advances in Communication, Network and computing – ICDeCom - 11, International Conference on “Devices & Communications”, Feb 24 – 25, 2011.BITS, Ranchi.

13. “Design and Implementation High Speed Memory in 130nm” - International Conference on Methods and Models in Science and Technology (ICM2ST-10) held at N I T T R – CHANDIGARH, Dec 25th - 26th , 2010

14. “Deep Sub-Micron SRAM Design for Low Leakage” in IEEE - ICCCT 2010 held at MNNIT - Allahabad, 17th – 19th September 2010.

National:

1. “Design of a different logic style address decoders for SRAM Memory Blocks”, National Conference on Smart Energy, VLSI and Embedded Systems, NCSEVES-2021, at JSSATE, Noida on 24th Sept 2021.

2. “Analysis of solar PV array based buck convertor design by using modified P&O Algorithm”, National Conference on Smart Energy, VLSI and Embedded Systems, NCSEVES-2021, at JSSATE, Noida on 24th Sept 2021.

3. “Electrical Intelligence Based Smart Yield Improvement”, National Conference on Smart Energy, VLSI and Embedded Systems, NCSEVES-2021, at JSSATE, Noida on 24th Sept 2021.

4. “Optimizing power and delay in reconfigurable memory by means of configurable selective pre-charge schemes", IEEE sponsored National conference on sustainable growth in Microelectronics and Communication Engineering, NCSMCE-2019, ABESEC, Ghaziabad, 28th May 2019.

5. “Design and Analysis of Optimum Performance Memory Decoders” October 12^{th} -14^{th}, NCVDES -2011, CSIR-CEERI Pilani.

6. “Decomposition of FSM into sub-state machines for reducing power”, 24^{th} – 25^{th} SPIN – 2011, AMITY, Noida.

7. “DRV analysis of Deep Sub-Micron SRAM Design for Low Leakage” – National conference on “Trends in VLSI Design & Embedded Systems” – held at KIIT, Gurgaon – 22^{nd} Jan 2010.

8. “Low power reduction techniques in CMOS through Improved Integer Linear Programming” - National Conference on Electronics – An indispensable tool for smart product innovations held at BBDIT – Ghaziabad – April 2007.

iv. Workshops /Conferences Attended

Designing and Modeling of IoT, AI & ML Systems, 1st to 6th August 2022, (1 Week), organized by AICTE -ATAL Academy, Arm Education and STMicroelectronics.
Advancements in Wireless Communications & Signal Processing - Leaping towards 5G, 26th to 31st July 2021, (1 Week), Dept. of ECE, JIIT, Noida.
Nascent Methodologies, Challenges and Realms of Research, 03 to 07 October 2020, (1 Week), Department of Electronics and Communication Engineering, Delhi Technological University, Delhi.
Solar PV and Storage Systems, 14th to 19th December 2020, (1 Week), Dept of EEE, JSSATE, Noida.
53 Online Webinars attended and 05 invited expert talks contributed in online webinars since March 2019 onwards.
AICTE sponsored “7 days FDP on Student Induction Program”, at SCEM, Mangaluru from 18th to 24th June 2019.
AKTU, Lucknow sponsored one-week FDP on “Analog Integrated Circuit Design Using Cadence Analog Design Flow “at JSSATE, Noida from 27th August 2018 to 1st September 2019.
Participated in one month (17th December 2018 to 12th January 2019) industrial training on “MITS PCB Prototyping Machine” at Entuple Technologies Private Limited, Bangalore.

FDP on “Working on Design and Implementation of Student Centre Learning” on 13th& 14th Jan 2016 at JSSATE, Noida.
“MOC Exchange Program” organized by Texas Instruments during 22 & 24th of Dec 2015 at AKTU, Luknow.
FDP on “Analog integrated circuits using CADENCE Analog Design Flow” from 7th to 11th Dec 2015 at Entuple Technologies Pvt Ltd, Bengaluru.
Workshop on “Wireless Sensor Networks using NetSim” on 28th& 29th Oct 2015 at JSSATE, Noida.
FDP on “Human Resource & Professional Ethics” on 20th Sep 2015 at JSSATE, Noida.
FDP on "ICT Based on VLSI Design" by NITTTR Chandigarh, at JSSATE Noida.
Training on "Integrated Projects and Design into Engineering Course" at JRE School of Engineering, Greater Noida, 16th July 2015
Training on "Calibration of Equipment by Fluke Technologies" at New Delhi on 18th March 2015.
Workshop on “India Microprocessor” at CDAC, Noida on 15th October 2014
Synopsys University Symposium, Delhi on 07 March 2014
Workshop on “Embedded System” on 22nd Sept 2012, JSSATEN.

v. Workshops / Conference (Organized)

Sl. No.	Name of the workshop / Conference	Organized by	Date	Role
-	-	-	-	-

vi. Conference Attended (those sponsored by AICTE / ISTE/IETE/TEQIP or any other sponsoring body)

Sl. No.	Name of the workshop / Conference	Organizer	Date
-	-	-	-

9. Details of NPTEL / COURSERA courses completed

Sl. No.	Name of the subject	Organized by	Date of completion / Award	Grade / Marks

1	CMOS Digital VLSI Design	NPTEL	2020	89%
2	NBA Accreditation and Teaching – Learning in Engineering (NATE)	NPTEL	2020	93%
3	Outcome Based Education and Digitisation	iNurture	2019	A+

10. Membership of Professional Bodies:

1. VLSI Society of India – Life Membership
2. IAENG – Life Membership

11. Any other information you will like to share about your professional experience

Industry Grants:

1. Texas Instruments (TI) – Analog and Embedded Technologies: TI – Sapience Consulting Sponsored Hardware Equipment's / Boards & Software's – TI-Nspire CX, TI-NSpire CXCAS & TI Connect **worth of Rs. 20 Lakhs.**

2. e-Yantra – Embedded Systems & Robotics: MHRD sponsored project under the National Mission for Education in ICT (NMEICT) program sponsored Hardware Equipment's **worth of Rs. 5 Lakhs.**